COMPUTER FOR EXECUTION OF TWO INSTRUCTION SETS

ABSTRACT

A computer is disclosed. The computer has a general register file of registers, a RISC instruction decoder, and a CISC instruction decoder. The RISC instruction decoder is exposed for execution of user-state programs in a RISC instruction set, being an instruction set having fixed-length instructions and a load/store/operate organization. The hardware CISC instruction decoder is exposed for execution by user-state programs in a CISC instruction set, being an instruction set with variable-length instructions and many instructions having multiple side-effects. The CISC decoder is designed to decode a portion of an instruction set for the computer, and to deliver the decoded instructions to an instruction execution pipeline designed to execute the output of both the RISC instruction decoder and the CISC instruction decoder. A software emulator is programmed to implement a remainder of the instruction set. The CISC instruction set provides accessibility to only a subset of the registers of the general register file, intermediate results of instructions of the instruction set being stored in registers of the general register file that are inaccessible in the CISC instruction set.